

Digital System Design

Add $\hookrightarrow R_x, R_y$

$$[R_x] + [R_y] \rightarrow R_x$$

in order for this to happen.

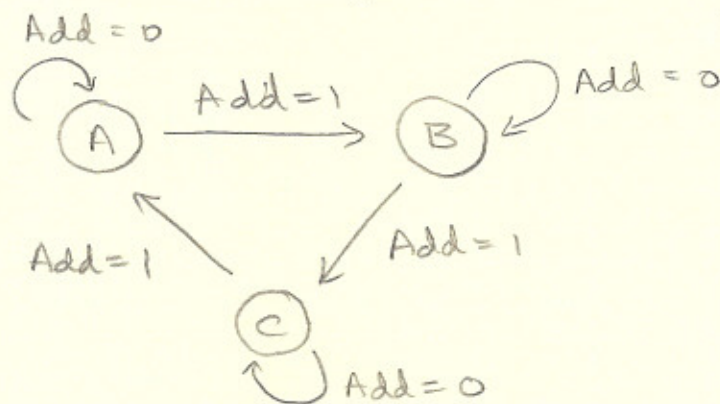
$$t+1 : R_{xout} = 1, R_{yout} = 1$$

$$t+2 : R_{Rout} = 1, R_{yout} = 1, R_B = 1, R_{cin} = 1$$

$$t+3 : R_{cout} = 1, R_{xin} = 1$$

This can all be represented by a Sequential Circuit (Synchronous)

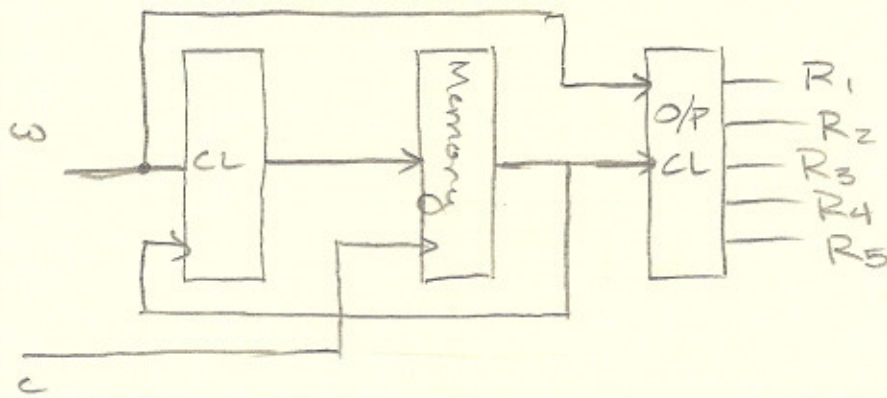
Add-0 state diagram.



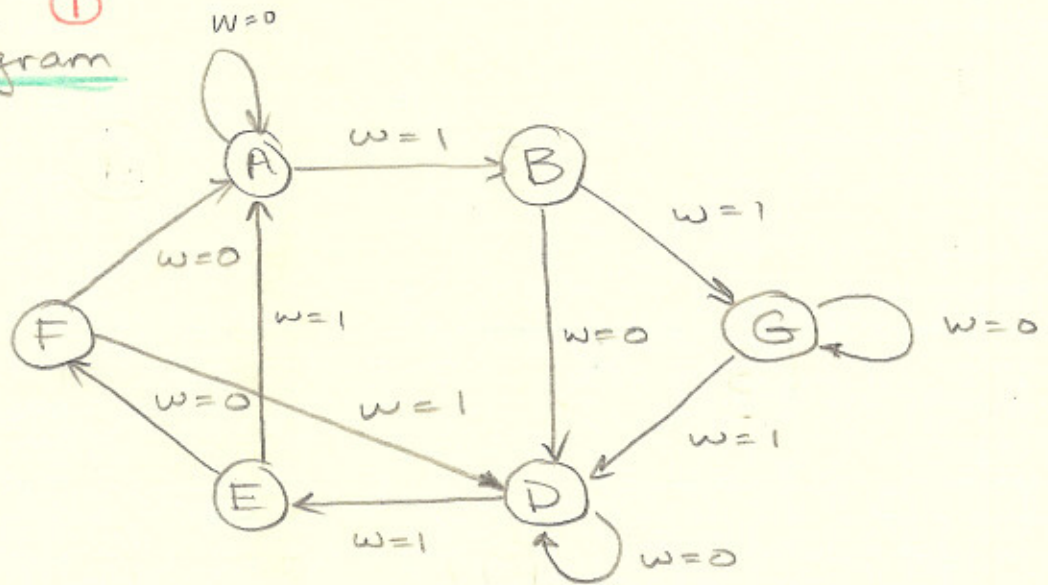
state A corresponds to $t+1$

B $t+2$

C $t+3$



State Diagram ①



State Table ②

Current State	w state		Out Puts				
	0	1	R ₁	R ₂	R ₃	R ₄	R ₅
A	A	B	1	1	0	0	0
B	D	C	1	1	0	1	0
C	C	D	0	0	1	0	0
D	D	E	1	1	1	1	0
E	F	A	0	1	0	1	0
F	A	D	0	0	1	0	0

State Assignment (3)

State	y_2	y_1	y_0
A	0	0	0
B	0	0	1
C	0	1	0
D	0	1	1
E	1	0	0
F	1	0	1
X	1	1	0
X	1	1	1

} there is no correspond states / bits.

State Assignment table (4)

Current State			next State			State			Outputs				
$w=1$	$w=0$		$w=1$	$w=0$		$w=1$	$w=0$		R_1	R_2	R_3	R_4	B_5
y_2	y_1	y_0	y_2	y_1	y_0	y_2	y_1	y_0					
0	0	0	0	0	0	0	0	1	1	1	0	0	0
0	0	1	0	1	1	0	1	0	1	1	0	1	0
0	1	0	0	1	0	0	1	0	0	0	1	0	0
0	1	1	0	1	1	1	0	0	1	1	1	1	0
1	0	0	1	0	1	0	0	0	0	1	0	1	0
1	0	1	0	0	0	0	0	1	0	0	1	0	0

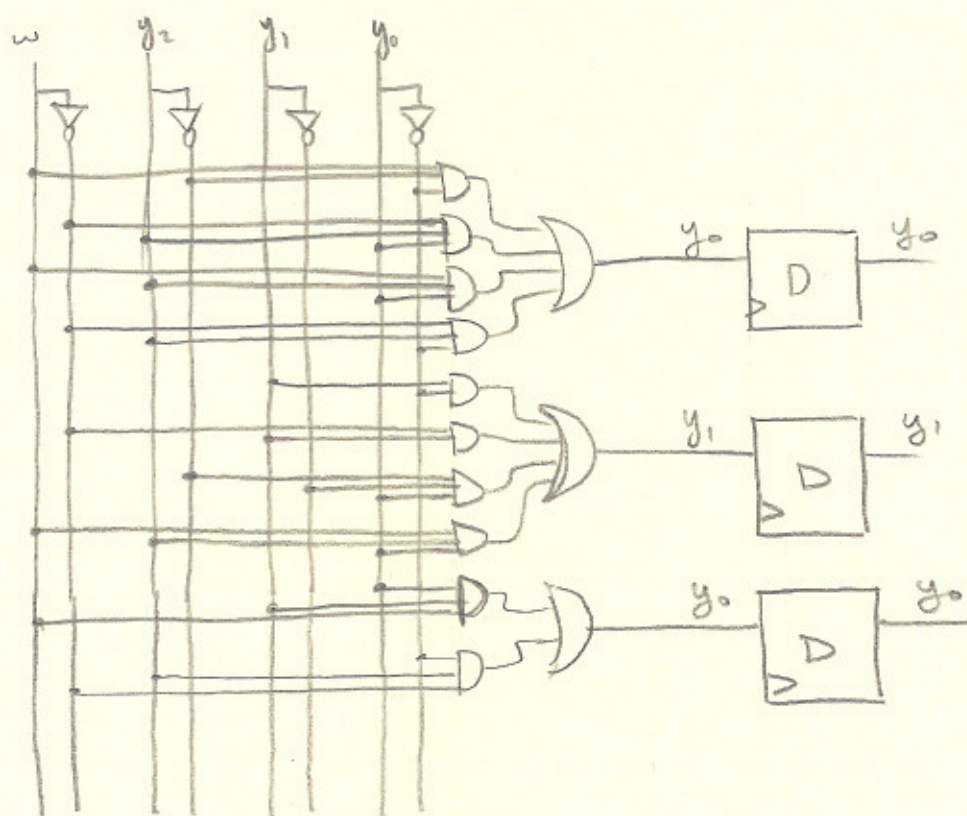
Kernal Map (5)

w				y_0	
y_2	0	1	0	1	y_1
	X	X	X	X	
	1	0	1	0	
	1	0	1	0	
				y_0	

$$y_0 = w \cdot \bar{y}_2 \cdot \bar{y}_0 + \bar{w} \cdot \bar{y}_2 \cdot y_0 + w \cdot y_2 \cdot y_0 + y_2 \cdot \bar{w} \cdot \bar{y}_0$$

Complete the other 2 kernal maps.

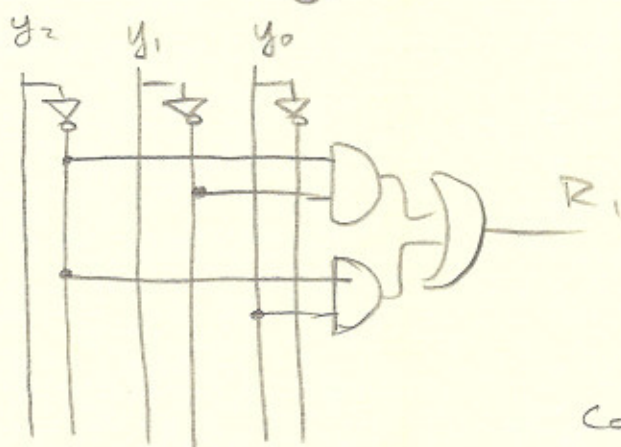
Design



Input CC (6)

	y_2			
y_1	x	x	1	
			1	1
	y_0			

$$R_1 = \overline{y_2} \cdot \overline{y_1} + \overline{y_2} \cdot y_0$$



Continue in a similar manner for $R_2 \rightarrow R_5$